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For Immediate Release

Cypress Samples World's Largest CPLDs

Delta39K™ CPLDs Offer Ease of Use, Performance and Non-Volatility
With Up to 350,000 Gates to Support High-Performance Communications Applications

SAN JOSE, Calif., November 6, 2000 – Cypress Semiconductor (NYSE: CY) today announced the availability of samples for the world's largest complex programmable logic devices (CPLDs). The Delta39K™ family offers more embedded memory – 240 Kbits for the 100,000-gate Delta39K100 – than any other programmable logic device (PLD), and is the first PLD to embed integrated FIFO and dual-port memories.

Delta39K CPLDs are offered with a pin-to-pin propagation delay as low as 6.5ns and true in-system performance up to 250 MHz. The devices are manufactured using a 0.18 micron, six-layer metal process, the most aggressive process ever used for a PLD. Innovative package options include an embedded non-volatile Flash memory die with the Delta39K die, creating a unique non-volatile solution and eliminating the need for an external boot PROM. Each device in the Delta39K family includes a programmable, Spread Aware™ phase locked loop (PLL) – with unmatched multiply, divide and clock edge control options – provides four global clocks to all logic clusters, memories and I/O cells to maintain precise on- and off-chip timing.

"Delta39K CPLDs showcase the range of Cypress's engineering capabilities and intellectual property, combining programmable logic with PLL, memory, manufacturing, and process expertise into a family of programmable communications devices," said Geoff Charubin, director of marketing for Cypress's data communications division. "Cypress is delivering a programmable solution with the advantages our CPLDs are known for: high speed, predictable timing, ease of use, and non-volatility at leadership densities."

"The Delta39K family of programmable logic devices are key components in the product portfolios we present to our customers in the wide area networking, storage networking and wireless infrastructure markets," said Scott Harmel, Cypress's director of corporate marketing. "Approximately

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three-quarters of Cypress's revenue is derived from communications markets, and this leading-edge programmable logic family strengthens our system solution capability."

About Delta39K CPLDs

The Delta39K architecture consists of logic block clusters (LBCs), each of which has 128 macrocells – eight 16-cell macrocell logic blocks – connected by a Programmable Interconnect Matrix™ (PIM™). Each LBC has 16 Kbits of single-port SRAM cluster memory, configurable as synchronous or asynchronous and as x1, x2, x4, or x8. The cluster memory can be cascaded with other cluster memory blocks to implement larger memory functions.

In addition to cluster memory blocks, each LBC has an associated channel memory block. The 4 Kbit channel memory uses Cypress's true-dual-ported cell to offer optimized dual-port and FIFO memory with completely independent write and read clocks. Each channel memory block includes FIFO control and the dual-port arbitration logic needed to implement extremely fast and powerful specialty memory functions. The Delta39K device will offer FIFO performance as high as 200 MHz. The channel memory, like the cluster memory, is configurable as x1, x2, x4, or x8 and its width and depth can be expanded.

The LBCs and channel blocks communicate through abundant vertical and horizontal routing channels. These channels also connect to a block of I/O pins at each end to provide maximum pinout flexibility and true In-System Reprogrammability™ (ISR™). ISR gives designers the flixibility to change a design with the confidence that speed and pinout will not be altered.

Software Support

The Delta39K CPLDs will be supported by Cypress's *Warp*™ design tools. The tools accept VHDL and Verilog HDL as input, and perform synthesis, technology mapping and fitting in one easy-to-use design environment. *Warp* features an architecture viewer, graphic timing analyzer and full LPM support to implement custom memory blocks. If a memory block is not specifically utilized by the designer, *Warp* software will automatically use it to implement large clusters of logic, increasing the effective density of a Delta39K device by more than 20 percent.

Delta39K Pricing

The Delta39K family spans eight device densities, ranging from 50,000 to 350,000 gates. Volume pricing in 2001 for the 100,000-gate Delta39K100 device – the first device being sampled – starts at $36.00.

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About Cypress

Cypress Semiconductor is “Driving the Communications Revolution”™ by providing high-performance integrated circuit solutions to fast-growing markets, including data communications, telecommunications, computation, consumer products, and industrial control. With a focus on emerging communications applications, Cypress's product portfolios include networking-optimized and micropower static RAMs; high-bandwidth multi-port and FIFO memories; high-density programmable logic devices; timing technology for PCs and other digital systems; and controllers for Universal Serial Bus (USB). Cypress is No. 1 in the USB and clock chip markets.

More than two-thirds of Cypress's sales come from fast-growing communications markets and dynamic companies such as Alcatel, Cisco, Ericsson, Lucent, Motorola, Nortel Networks, and 3Com. Cypress’s ability to mix and match its broad portfolio of intellectual property enables targeted, integrated solutions for high-speed systems that feed bandwidth-hungry Internet applications. Cypress aims to become the preferred silicon supplier for Internet switching systems and for every Internet data stream to pass through at least one Cypress IC.

Cypress employs more than 4,100 people worldwide with international headquarters in San Jose, California. Its shares are listed on the New York Stock Exchange under the symbol CY. More information about Cypress is accessible electronically on the company's worldwide Web site at http://www.cypress.com or by CD-ROM (call 1-800-858-1810). An electronic investor forum, and other investor information, is located at http://www.cypress.com/investor/index.html.

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